US009543425B2

(12) **United States Patent**
Khan et al.

(10) **Patent No.: US 9,543,425 B2**
(45) **Date of Patent: Jan. 10, 2017**

(54) **MULTI-FINGER LARGE PERIPHERY ALINN/ALN/GAN METAL-OXIDE-SEMICONDUCTOR HETEROSTRUCTURE FIELD EFFECT TRANSISTORS ON SAPPHIRE SUBSTRATE**

(71) Applicant: **University of South Carolina**, Columbia, SC (US)

(72) Inventors: **Asif Khan**, Irmo, SC (US); **Vinod Adivarahan**, Columbia, SC (US)

(73) Assignee: **University of South Carolina**, Columbia, SC (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **15/137,078**

(22) Filed: **Apr. 25, 2016**

(65) **Prior Publication Data**

US 2016/0240647 A1 Aug. 18, 2016

Related U.S. Application Data

(62) Division of application No. 14/666,768, filed on Mar. 24, 2015, now Pat. No. 9,343,544.

(60) Provisional application No. 61/969,491, filed on Mar. 24, 2014.

(51) **Int. Cl.**

H01L 21/338	(2006.01)
H01L 29/778	(2006.01)
H01L 29/66	(2006.01)
H01L 29/20	(2006.01)
H01L 29/205	(2006.01)
H01L 29/78	(2006.01)
H01L 29/417	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 29/7787*** (2013.01); ***H01L 29/2003*** (2013.01); ***H01L 29/205*** (2013.01); ***H01L 29/66462*** (2013.01); ***H01L 29/66484*** (2013.01); ***H01L 29/66522*** (2013.01); ***H01L 29/7786*** (2013.01); ***H01L 29/7831*** (2013.01); *H01L 29/41758* (2013.01)

(58) **Field of Classification Search**

CPC H01L 29/2003; H01L 29/66462; H01L 29/7787; H01L 29/205

USPC 438/172; 257/76, 194

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

2006/0202272 A1*	9/2006	Wu	.....	H01L 29/7787 257/355
2007/0228415 A1*	10/2007	Kanamura	.....	H01L 29/2003 257/192

* cited by examiner

Primary Examiner — Theresa T Doan

(74) *Attorney, Agent, or Firm* — Dority & manning, P.A.

(57) **ABSTRACT**

MOSHFET devices are provided, along with their methods of fabrication. The MOSHFET device can include a substrate; a multilayer stack on the substrate; a ultra-thin barrier layer on the multilayer stack, wherein the ultra-thin barrier layer has a thickness of about 0.5 nm to about 10 nm; a dielectric, discontinuous thin film layer on portions of the ultra-thin barrier layer, wherein the dielectric, discontinuous thin film layer comprises SiO_2; a plurality of source electrodes and drain electrodes formed directly on the ultra-thin barrier layer in an alternating pattern such that the dielectric, discontinuous thin film layer is positioned between adjacent source electrodes and drain electrodes; a plurality of gate electrodes on the dielectric, discontinuous thin film layer; and a gate interconnect electrically connecting the plurality of gate electrodes.

12 Claims, 7 Drawing Sheets